



# A Software Tool for PCIe® 4.0 Rx Lane Margining

**Pelle Fornberg**  
**Sr. Staff Engineer**  
**Intel**

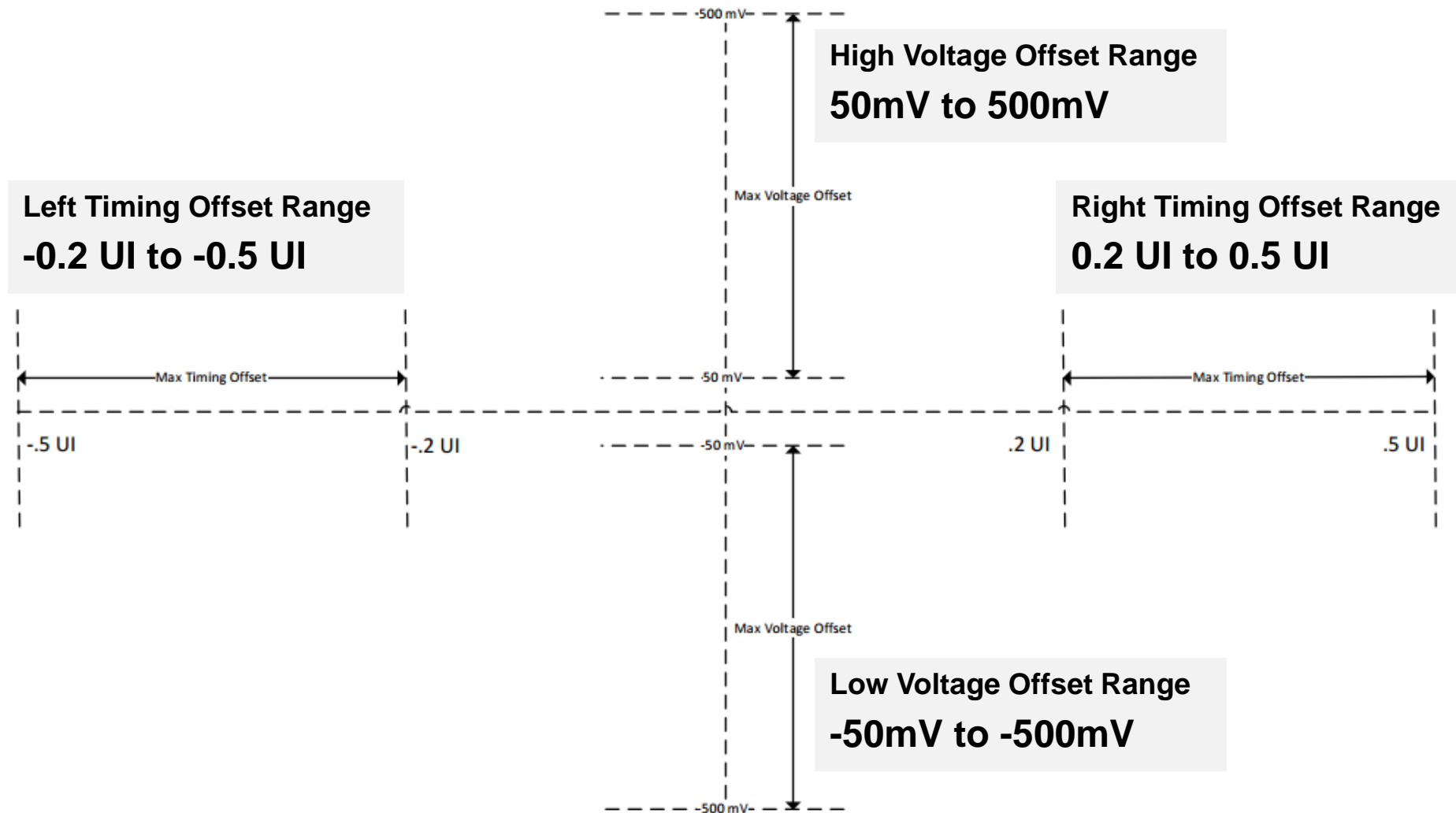
- **PCIe 4.0 Rx Lane Margining**
- **PCIe 4.0 Rx Lane Margining Tool**
  - Features
  - Current Status
- **Example Margin Results**
- **Deployment Plans**

# PCIe 4.0 Rx Lane Margining



- **New feature added to the PCIe 4.0 base spec**
- **Lane margining is mandatory for all ports that support 16 GT/s**
- **System SW obtains information for a given receiver while the Link is in L0**
- **Voltage margin (optional) and timing margin (mandatory)**
- **Independent timing margining is optional**

# PCIe 4.0 Rx Lane Margining



# PCIe 4.0 Rx Lane Margining Tool



- **Intel is developing a receiver margining tool to be offered to the PCI-SIG<sup>®</sup> for member use**
  - Developed using Python, source code to be provided
  - Can be used for a quick check of link segment electrical performance
  - Can identify poor performing lanes for detailed stress eye testing
- **The tool can margin the receivers on hosts, retimers, and endpoint devices**

- **The tool is under development**
  - Supports root ports and endpoints
  - Command line based, GUI in development
- **Tool demo provided at the June 2017 PCI-SIG Developers Conference in Santa Clara at the Synopsys booth**
- **Successfully obtained margins with multiple PCIe 4.0 capable endpoint devices at the April and August 2017 PCI-SIG Compliance Workshops in Milpitas**

- **Supports 2 different modes (Basic & Advanced)**
- **Basic Mode**
  - Margin all the receivers connected on the path
    - Margin upstream component (DSP)
    - Margin retimers (DSP and USP)
    - Margin downstream component (USP)
  - Port margining – All lanes to be margined
  - EW margining
  - EW margining per side – If implemented in silicon
  - EH margining – If implemented in silicon
  - Min dwell/BER per step using the spec minimum of  $10^8$

- **Advanced Mode**
  - Per lane margining
  - Control error threshold
  - Control dwell/BER
  - 2 dwell time options for reduced test time
  - Target specific receivers
  - Set max range for EW and EH – In steps
- **Command line & GUI**
- **Plan to test with the following OS's**
  - Windows10
  - Linux



# Basic Mode GUI Mockup

Test Mode

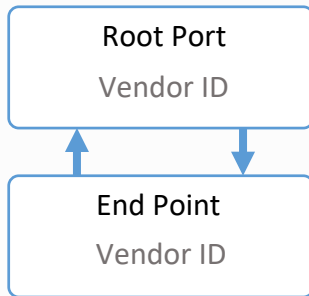
☒ Basic ☐ Advanced

Margin

Port  
Width  
Margin

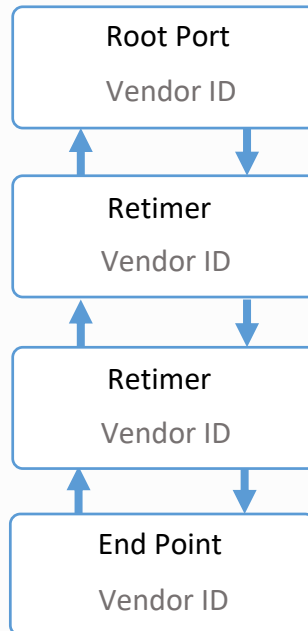
1

x1



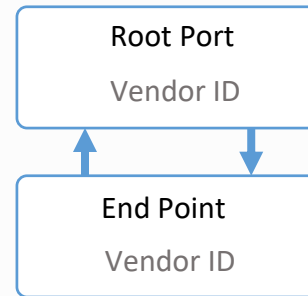
3

x16



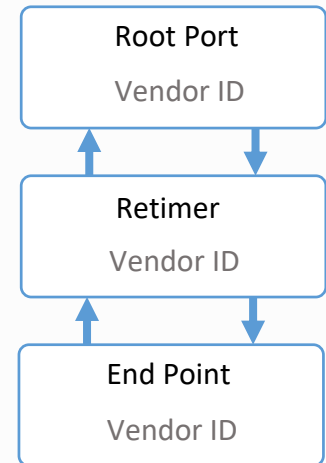
9

x4



14

x4



# Advanced Mode GUI Mockup



Test Mode ☐ Basic ☒ Advanced

Margin

Margin Type ☒ Port ☐ Lane

Max Voltage Limit 36

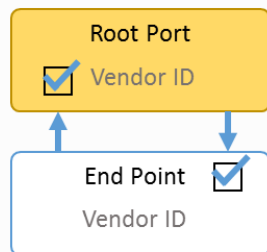
Dwell Time (s) 36

Max Timing Limit 16

Port  
Width  
Margin

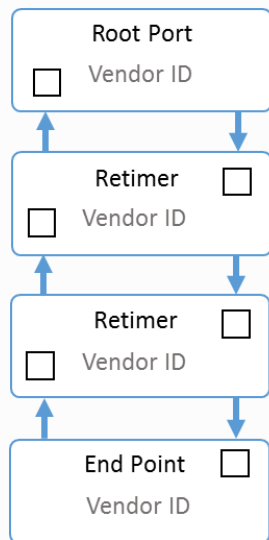
1

x1



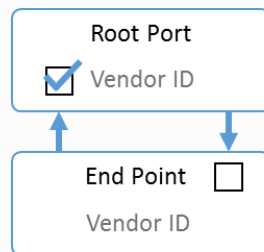
3

x16



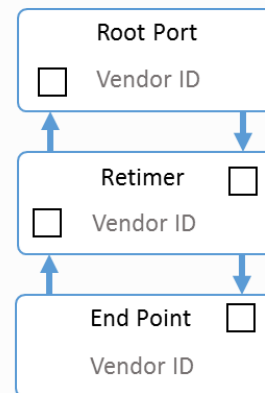
9

x4



14

x4



## Port 1: Root Port

Margin Capability	Voltage & Timing
Max Voltage Range	64 steps, 200 mV
Max Timing Range	32 steps, 0.5 UI
Independent TM	No
Independent VM	Yes
Bus	0
Device	1
Function	1
Device ID	007
Vendor ID	8086 (Intel)
Margin Lane 1	<input checked="" type="checkbox"/>
Margin Lane 2	<input checked="" type="checkbox"/>
Margin Lane 3	<input checked="" type="checkbox"/>
Margin Lane 4	<input checked="" type="checkbox"/>

# Early GUI Prototype

PCIe Gen. 4 Lane Margining Tool

File

Margin Type: ☒ Port ☐ Lane

Max Voltage Limit: 50 Dwell Time: 1

Max Timing Limit: 50 Error Count: 4

Back Launch Test

Margin ☒

Port 0

Width x4

Root Port

☒ R1 Vendor ID

Retimer ☐ R2

☐ R3 Vendor ID

Retimer ☐ R4

☐ R5 Vendor ID

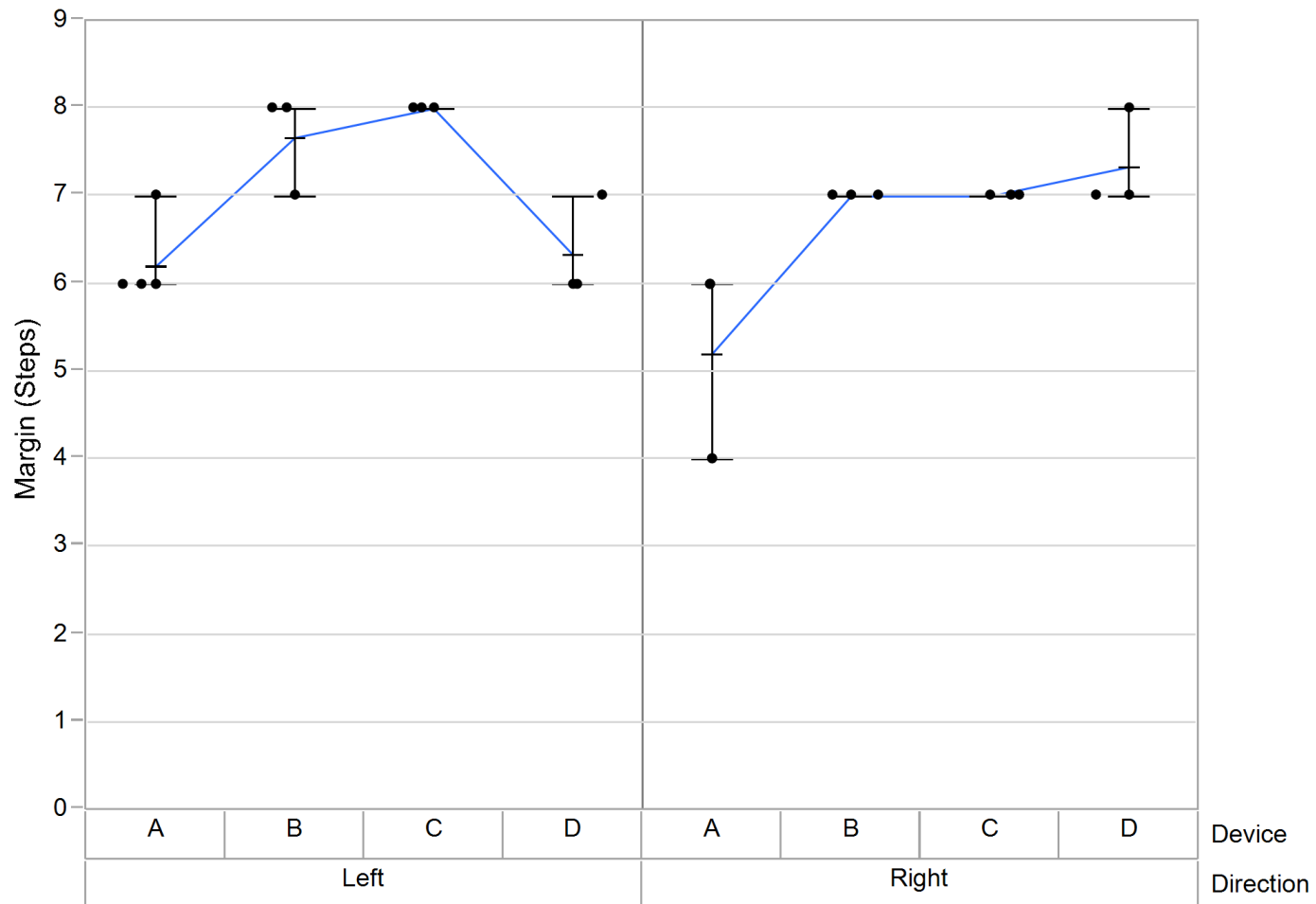
End Point ☐ R6

Vendor ID

Port 0: Receiver 4 & Port 0: Receiver 5

Margin Capability	Voltage & Timing
Max Voltage Range	64 steps, 200 mV
Max Timing Range	32 steps, 0.5 UI
Independent TM	No
Independent VM	Yes
Bus	0
Device	0
Function	0
Device ID	0x19a58088
Vendor ID	8088(Intel)

# Margining Example



# Deployment Plans



- **Intel plans to provide the source to the PCI-SIG**
- **All decision on whether it will be accepted or released is up to the PCI-SIG**

# Acknowledgements



**The following individuals have contributed to the development of this tool**

- **Victor Miguel Castillo**
- **Manisha Nilange**
- **Alec Zitzelberger**
- **Dan Froelich**
- **Tal Israeli**

**Thank you for attending the  
PCI-SIG Developers Conference Israel  
2017.**

**For more information please go to  
[www.pcisig.com](http://www.pcisig.com)**